IN THE CLAIMS

Presented below are all of the pending claims.

Claims 1-20. (Canceled)

21. (Previously presented) A system, comprising:

a bus;

a processor including a plurality of machine specific registers, wherein each one of the plurality of machine specific registers is associated with one or more functional units of the processor; and

a computer readable medium external to the processor and coupled to the processor by the bus, the computer readable medium to store instructions to implement microcode functions which result in changing a value of at least one bit in at least one of the plurality of machine specific registers.

22. (Currently amended) The system of claim 21 [[1]], wherein the computer readable medium is firmware.

23. (Currently amended) The system of claim 21 [[1]], wherein the plurality of machine specific registers includes a bank of registers associated with one of the functional units.

24. (Currently amended) The system of claim 21 [[1]], wherein one of the functional units is an internal bus controller.

25. (Currently amended) The system of claim 21 [[1]], wherein one of the functional units is an internal data cache of the processor.

26. (Previously presented) The system of claim 25, wherein the instructions implement microcode functions by updating the at least one of the plurality of machine specific registers.

27. (Previously presented) The system of claim 26, wherein the instructions implement microcode functions by setting the at least one bit to invalidate a line of the cache.

28. (Previously presented) The system of claim 25, wherein the instructions implement microcode functions by triggering processor hardware logic and by manipulating the plurality of machine specific registers.

29. (Previously presented) A method, comprising:

storing microcode on a computer readable medium external to a processor;

executing the microcode using the processor, wherein the processor includes a plurality of machine specific registers associated with at least two functional units of the processor; and

controlling one of the at least two functional units of the processor in response to executing the microcode by modifying a value of at least one bit included in one of the plurality of machine specific registers.

30. (Previously presented) The method of claim 29, wherein modifying a value of at least one bit included in one of the plurality of machine specific registers associated with one of the at least two functional units of the processor operates to affect the behavior of an other one of the at least two functional units of the processor.

31. (Previously presented) The method of claim 29, wherein a logical source register and a logical destination register for executing an instruction of the microcode are selected from the plurality of machine specific registers.

32. (Previously presented) The method of claim 29, wherein the at least two functional units are linked by a communication bus to a data control unit to fetch an instruction of the microcode from the computer readable medium external to a processor.

33. (Previously presented) The method of claim 29, wherein controlling one of the at least two functional units of the processor in response to executing the microcode further includes:

controlling a non-performance critical function.

34. (Previously presented) The method of claim 33, wherein the non-performance critical function is selected from the group consisting of:

cache flushing, cache invalidation, setting processor features, reading processor features, machine check handling, floating point calculations, processor diagnosis, architecture handling for backward compatibility, authentication, platform management interrupt, diagnostic functions and debug functions.

35. (Previously presented) An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

storing microcode in firmware external to a processor;

executing the microcode by the processor;

updating one or more machine specific registers associated with a logic unit on the processor in response to the executing of the programmed code; and

controlling one or more functions of the logic unit on the processor based on a value stored in the one or more machine specific registers.

36. (Previously presented) The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

moving a value from a general purpose register of the processor to the one or more machine specific registers.

37. (Previously presented) The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

reprogramming the microcode in the firmware.

38. (Previously presented) An apparatus, comprising:

a first logic unit; and

at least two machine specific registers associated with the logic unit, the at least two machine specific registers to trigger processor hardware logic functions when a selected one of the at least two machine specific registers is updated in response to executing a microcode instruction fetched from a memory external to the processor.

39. (Previously presented) The apparatus of claim 38, further comprising:

a second logic unit associated with a selected one of the at least two machine specific registers.

40. (Previously presented) The apparatus of claim 39, wherein changing a value of at least one bit in a selected other one of the at least two machine specific registers affects the behavior of the second logic unit.